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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,169	07/03/2003	Douglas R. Hackler SR.	51889/2	9150

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John R. Thompson
STOEL RIVES LLP
One Utah Center
201 South Main Street, Suite 1100
Salt Lake City, UT 84111

EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/613,169	HACKLER ET AL.
	Examiner	Art Unit
	Phat X. Cao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *5,6,9-16,21,22,42-43* is/are withdrawn from consideration.

5)☒ Claim(s) *34-41 and 44* is/are allowed.

6)☒ Claim(s) *1,4,7,8,17,20,23-28 and 31* is/are rejected.

7)☒ Claim(s) *2,3,18,19,29,30,32 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/03; 3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-4, 7-8, 17-20, 23-41 and 44 in the reply filed on 12/21/04 is acknowledged. The traversal is on the ground(s) that "the Office Action has not found any reasons for distinction as required". This is not found persuasive because as clearly stated in the last restriction requirement, Group I, Group II and Group III are different devices. One of ordinary skill in the art would have no difficulty to recognize that the double-gated device having four terminals (Group I) would be distinct from a lateral bipolar transistor device (Group II) or from a DTMOS device having three terminals (Group III). Therefore, Applicant fails to provide the reasons to support that the devices claimed in Group I, Group II and Group III as proposed by the examiner are not distinct.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 8 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al, "Super Self-Aligned Double-Gate (SSDG) MOSFETs Utilizing Oxidation Rate Difference and Selective Epitaxy", IEEE, pp. 3.5.1-3.5.4 (cited by Applicant).

Regarding claims 1 and 28, lee (Figs. (e')-(f')) discloses a field effect transistor,

comprising: a substrate; bottom gate control means BG disposed on the substrate for effecting gate control; a dielectric LTO disposed on the substrate; channel means (Si film) disposed above the bottom gate BG for providing an electron flow; a source disposed on the dielectric LTO and having a source extension extending from a main body of the source and coupled to the channel means; a drain disposed on the dielectric LTO and having a drain extension extending from a main body of the drain and coupled to the channel means; a gate dielectric insulator disposed on the channel means; a top gate control means TG disposed on the gate dielectric insulator for effecting gate control (also see Fig. 5); a first spacer disposed between the top gate control means TG and the source and proximate to the source extension; and a second spacer disposed between the top gate control means TG and the drain and proximate to the drain extension.

Regarding claim 8, Lee (Fig. (f')) further discloses that the main body of the source and the drain is vertically disposed higher than the channel (Si film).

4. Claims 1, 4, 7-8, 28 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumar et al (US. 6,248,626).

Regarding claims 1 and 28, Kumar (Figs. 4A-4F) discloses a substrate 40; bottom gate control means 45 disposed on the substrate 40 for effecting gate control; a dielectric 41 disposed on the substrate 40; channel means 48 disposed above the bottom gate 45 for providing an electron flow; a source disposed on the dielectric and having a source extension extending from a main body of the source and coupled to the channel means 48 (see Figs. 4E and 4F); a drain disposed on the dielectric and having

a drain extension extending from a main body of the drain and coupled to the channel means 48 (see Figs. 4E and 4F); a gate dielectric insulator 47 disposed on the channel means 48; a top gate control means G disposed on the gate dielectric insulator for effecting gate control; a first spacer 50 (left side) disposed between the top gate control means G and the source ad proximate to the source extension; and a second spacer 50 (right side) disposed between the top gate control means G and the drain and proximate to the drain extension.

Regarding claims 7-8, Kumar (Fig. 4E) further discloses that the channel 48 or layer 44 is undoped (i.e., silicon) (column 6, lines 8-11), and the main body of the source and drain is vertically disposed higher than the channel 48.

Regarding claims 4 and 31, as discussed in details above, Kumar (Figs. 4A-4F) reads on the above claims. Kumar (Fig. 4F) further discloses a first local interconnect coupled to the top gate and disposed between the first and second spacer 50; and a second local interconnect (not shown in Fig. 4F, see Figs. 2A and column 9, lines 14-20) insulated from the first local interconnect and coupled to the bottom gate to provide independent bias to the bottom gate.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4, 7-8, 17, 20, 23-27, 28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US. 2002/0093053) in view of Kumar et al (US. 6,248,626).

Regarding claims 1, 17 and 28, Chan (Figs. 1A-1C) discloses a field effect transistor, comprising: a substrate 4; a bottom gate (not labeled) disposed on the substrate 4; a dielectric 3 disposed on the substrate; a channel 5 disposed above the bottom gate; a source 9 disposed on the dielectric 3 and coupled to the channel 5; a drain 9 disposed on the dielectric 3 and coupled to the channel 5; a gate insulator 11 disposed on the channel (see Fig. 2W); a top gate 12 disposed on the gate insulator; a first insulating spacer 11 (corresponding to a portion of an insulating layer 11 formed on a left sidewall of the top gate 12) (see Fig. 2AA and par. [0073]) disposed between the top gate 12 and the source 9 and proximate to the channel 5; a second insulating spacer 11 (corresponding to a portion of an insulating layer 11 formed on a right sidewall of the top gate 12) (see Fig. 2AA and par. [0073]); a local interconnect 14 disposed on the top gate 12 and between the first and second spacers 11 (see Fig. 1B); a first insulating pad 11 (corresponding to a portion of an insulating layer 11 formed on a top surface of the source 9) disposed on the source 9; a second pad 11 (corresponding to a portion of an insulating layer 11 formed on a top surface of the drain 9; a first contact 15 extending through the first pad and coupled to the source 9; and a second contact 15 extending through the second pad and coupled to the drain 9.

Chan does not disclose the source/drain 9 having the source/drain extensions.

However, Kumar (Figs. 4E and 4F) teaches the forming of a dual-gate device comprising the source/drain disposed on a dielectric and having source/drain extensions extending under the top gate and coupled to the channel 48. Accordingly, it would have been obvious to modify the transistor of Chan by forming the source/drain 9 with the source/drain extensions as suggested because such source/drain extensions are well known and commonly used for preventing the short channel effect of the transistor.

Regarding claims 4, 20 and 31, Chan does not specifically disclose a second local interconnect coupled to the bottom gate. However, Kumar (Fig. 2A) further teaches the forming of a first local interconnect coupled to the top gate, and the forming of a second local interconnect insulated from the first local interconnect and coupled to the bottom gate to provide independent bias to the bottom gate. Accordingly, it would have been obvious to couple a second local interconnect to the bottom gate of Chan because as taught by Kumar, such top gate and bottom gate interconnects would form the logic transistors (column 6, lines 59-62).

Regarding claims 7-8 and 23-24, Chan's Fig. 1A further discloses that the channel 5 is undoped (i.e., SOI) and the main body of the source/drain 9 is vertically disposed higher than the channel 5.

Regarding claims 25-26, Chan (Fig. 2W) further discloses: a plurality of exterior spacers 11 disposed on the sidewalls of source/drain 9 and proximate to the dielectric layer 3, source/drain 9 and pads (corresponding to the portions of an insulating layer 11

formed on the top surfaces of source/drain 9); and an insulator 13 (Fig. 1A) disposed on the substrate and coupled to the exterior spacers 11.

Regarding claim 27, Chan (Fig. 1A) further discloses an ILD layer 13 disposed on the first and second pads 11 and wherein first and second contacts 15 extend through the ILD layer 13.

7. Claims 1, 4, 8, 17, 20, 24-27, 28, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parke (US. 6,580,137) in view of Hanafi et al (US. 2002/0105039).

Regarding claims 1, 17 and 28, Parke (Figs. 12B and 12C) discloses a field effect transistor, comprising: a substrate 11; a bottom gate 124' disposed on the substrate; a dielectric 13 disposed on the substrate 11; a channel 122 disposed above the bottom gate 124'; a source 114s disposed on the dielectric and coupled to the channel; a drain 114d disposed on the dielectric and coupled to the channel; a gate dielectric insulator 128 disposed on the channel; a top gate 130 disposed on the gate dielectric insulator; a first insulting spacer 30 disposed between the top gate 130 and the source 114s and proximate to the channel 122; a second insulating spacer 30 dispose between the top gate 130 and the drain 114d and proximate to the channel; a local interconnect 140 disposed on the top gate 130 and between the first and second spacers 30; a first pad 20 (not labeled, see Fig. 11B) disposed on the source 114s; a second pad 20 (also see Fig. 11B) disposed on the drain 114d; a first contact 222 extending through the first pad and coupled to the source 114s; and a second contact 222 extending through the second pad and coupled to the drain 114d.

Parke does not disclose the source/drain 114 having the source/drain extensions.

However, Hanafi (Fig. 10) teaches the forming of a dual-gate device comprising the source/drain disposed on a dielectric 24 and having source/drain extensions 32 extending under a top gate 46 and coupled to the channel 40. Accordingly, it would have been obvious to modify the transistor of Parke by forming the source/drain 114 with the source/drain extensions as suggested because such source/drain extensions are well known and commonly used for preventing the short channel effect of the transistor.

Regarding claims 4, 20 and 31, Parke (Fig. 13C) further discloses the forming of a second local interconnect 234 insulated from the first local interconnect 140 and coupled to the bottom gate 124' to provide independent bias to the bottom gate.

Regarding claims 8 and 24, Parke (Fig. 12B) further discloses that the main body of the source/drain 114 is vertically disposed higher than the channel 124'.

Regarding claims 25-27, Parke (Fig. 12B) further discloses: a plurality of exterior spacers 30 (not labeled, see Fig. 13B) disposed on the substrate 11 and proximate to the dielectric layer 13, source/drain 144 and pads 20; an insulator layer 40 (Fig. 9B) disposed on the substrate and coupled to the exterior spacers 30; and an ILD layer 210 disposed on the first/second pads 20 and wherein the first/second contacts 222 extend through the ILD layer 210.

Allowable Subject Matter

8. Claims 2-3, 18-19, 29-30 and 32-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose the channel has a cross-section U-shape.

9. Claims 34-41 and 44 are allowed.

The prior art of record fails to disclose a plurality of nitride exterior spacers disposed on the substrate and surrounding the bottom gate, dielectric, source/drain, gate insulator and top gate.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
March 14, 2005

PHAT X. CAO
PRIMARY EXAMINER